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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/687,540	10/13/2000	Keith Balmer	TI-26011	8915

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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.

EXAMINER

ART UNIT	PAPER
	6

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Commissioner for Patents

The reply filed on 3/11/04 is not fully responsive to the prior Office Action because of the following omission(s) or matter(s): The examiner objected to the drawings under 37 CFR 1.83(a) because they failed to show Fig. 9 as described in the specification on page 19, line 29 through page 20, line 6. A proposed drawing correction or corrected drawings were required in reply to the Office action to avoid abandonment of the application. Applicants were also told the objection to the drawings would not be held in abeyance. Possibly, applicants' specification and/or drawings do not match those in the examiner's possession. Therefore, the examiner is supplying applicants with a copy of his version of Figure 9 and the description of it found in his specification. See 37 CFR 1.111. Since the above-mentioned reply appears to be *bona fide*, applicant is given **ONE (1) MONTH or THIRTY (30) DAYS** from the mailing date of this notice, whichever is longer, within which to supply the omission or correction in order to avoid abandonment. EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136(a).

WILLIAM M. TREAT
PRIMARY EXAMINER

which is shared with source 4 of S unit group **82**, is used for Extended Multiply (EMPY) instructions. Multiplier **126** in M unit group **84** has 3 pipeline stages and no hotpath. The first 2 stages perform array multiplication in a carry/sum format. The last stage performs carry propagate addition and produces up to a 64-bit result. The 64-bit result is written back to RF **76** in pairs. Galois multiply hardware resides in M-unit group **84** alongside the main multiplier array, and it also takes 3 cycles. P unit group **74** operates just like the A, C, and S unit groups, except that it has no hotpath and that its result is consumed by the program control logic in the fetch unit instead of being written back to RF **76**. P unit group **74** only has one operand port which is shared with source 2 of A unit group **78**, which precludes parallel execution of a branch instruction and any instruction in A unit group **78**.

Figs. **8** - **14** are block diagrams illustrating more detail of the operation and hardware configuration of each of the unit groups within the DSP core. Fig. **8** is a top level diagram of fetch unit **60**, which consists primarily of Program Counter **126** and other components generally responsible for controlling program flow, and the majority of control registers not directly related to the operation of a specific unit. With respect to program flow, fetch unit **60** has two main modes of operation: normal (sequential) operation and branch operation. Additionally, fetch unit **60** must initiate any interrupt/exception handling, resets, and privilege-level changes for DSP core **44**.

Fig. **9** is a top-level temporal block diagram of Register File **76**. Within each DSP core **44** there are two datapaths, A **68** and B **70**, each containing an identical

register file. As used herein, the registers in the A (B) datapath are denoted by a0, ..., a31 (b0, ..., b31). Each register file **76** is composed of thirty-two 32-bit registers configured in upper and lower banks of 16 registers each. There are 12 read ports and 6 write ports for each register file **76**.

Fig **10** is a top level block diagram of A unit group **78**, which supports a portion of the arithmetic and logic operations of DSP core **44**. A unit group **78** handles a variety of operation types requiring a number of functional units including A adder unit **128**, A zero detect unit **130**, A bit detection unit **132**, A R/Z logic unit **134**, A pack/replicate unit **136**, A shuffle unit **138**, A generic logic block unit **140**, and A div-seed unit **142**. Partitioning of the functional sub-units is based on the functional requirements of A unit group **78**, emphasizing maximum performance while still achieving low power goals. There are two input muxes **144** and **146** for the input operands, both of which allow routing of operands from one of five sources. Both muxes have three hotpath sources from the A, C and S result busses, and a direct input from register file **76** in the primary datapath. In addition, src1 mux **144** can pass constant data from decode unit **62**, while src2 mux **146** provides a path for operands from the opposite datapath. Result mux **148** is split into four levels. Simple operations which complete early in the clock cycle are pre-muxed in order to reduce loading on the critical final output mux. A unit group **78** is also responsible for handling control register operations **143**. Although no hardware is required, these operations borrow the read and write ports of A unit group **78** for routing data. The src2 read port is used to

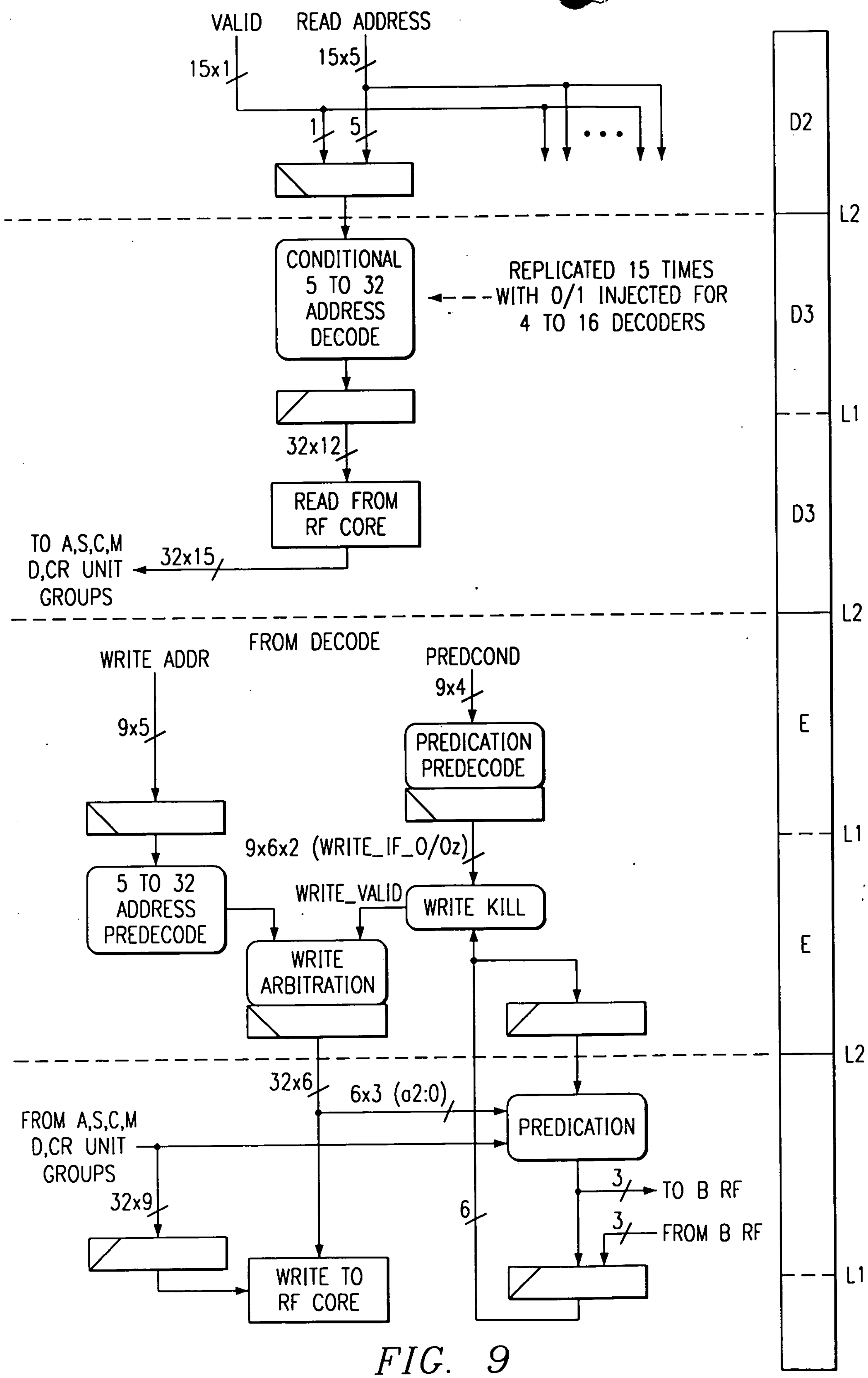
VALID
READ ADDRESS
15x1
15x5
1
5
CONDITIONAL 5 TO 32 ADDRESS DECODE
REPLICATED 15 TIMES WITH 0/1 INJECTED FOR 4 TO 16 DECODERS
32x12
READ FROM RF CORE
TO A,S,C,M D,CR UNIT GROUPS
32x15
FROM DECODE
WRITE ADDR
PREDCOND
9x4
9x5
PREDICATION PREDECODE
9x6x2 (WRITE_IF_0/0z)
5 TO 32 ADDRESS PREDECODE
WRITE_VALID
WRITE KILL
WRITE ARBITRATION
32x6
6x3 (a2:0)
FROM A,S,C,M D,CR UNIT GROUPS
PREDICATION
3
TO B RF
32x9
6
3
FROM B RF
WRITE TO RF CORE
D2
L2
D3
L1
D3
L2
E
L1
E
L2
L1

FIG. 9